Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.An electrically erasable programmable read only memory (EERPOM) with source line voltage stabilization mechanism, comprising:

a semiconductor substrate of a first conductivity type having a memory region;

a deep ion well of a second conductivity type formed in said semiconductor substrate;

a cell ion well of said first conductivity type located within said memory region in said semiconductor substrate, said cell ion well being situated above said deep ion well;

a shallow ion well of said second conductivity type serving as a buried bit line doped within said cell ion well, said shallow ion well being isolated by an STI layer, wherein said STI layer has a thickness greater than a well depth of said shallow ion well;

at least one memory transistor comprising a stacked gate, a source, and a drain formed on said shallow ion well, wherein said source of said memory transistor is electrically coupled to said cell ion well to induce a capacitor between said cell ion well and said deep ion well

during a read operation, thereby avoiding read current bounce or potential power crash; and

a bit line overlying said memory transistor and electrically connected to said drain of said memory transistor via a bit line contact plug short-circuiting said drain of said memory transistor and said shallow ion well.

[c2] 2.The EERPOM according to claim 1 wherein said first conductivity type is N type and said second conductivity type is P type.

[c3] 3.The EERPOM according to claim 1 wherein said stacked gate of said memory transistor comprises a floating gate and a control gate stacked on said floating gate.

[c4] 4.The EERPOM according to claim 3 wherein said control gate of said memory transistor is electrically connected to a word line.

[c5] 5.The EERPOM according to claim 1 wherein during said read operation, a positive read voltage is applied on said source line, and said deep ion well is grounded.

[c6] 6.An electrically erasable programmable read only memory (EERPOM) with source line voltage stabilization mechanism, comprising:

a semiconductor substrate of a first conductivity type having a memory region;

a deep ion well of a second conductivity typeformed in said semiconductor substrate;

a cell ion well of said first conductivity type located within said memory region in said semiconductor substrate, said cell ion well being situated above said deep ion well;

a shallow ion well of said second conductivity type serving as a buried bit line doped within said cell ion well, said shallow ion well being isolated by an STI layer, wherein said STI layer has a thickness greater than a well depth of said shallow ion well;

at least one memory transistor comprising a stacked gate, a source, and a drain formed on said shallow ion well;

a selection transistor formed on said shallow ion well, said selection transistor has a first terminal serially connected to said source of said memory transistor, said selection transistor comprising a select gate and a second terminal electrically coupled to a source line, wherein said source line is electrically coupled to said cell ion well to induce a capacitor between said cell ion well and said deep ion well during a read operation, thereby avoiding read current bounce or potential power crash; and

a bit line overlying said memory transistor and electrically connected to said drain of said memory transistor

via a bit line contact plug short-circuiting said drain of said memory transistor and said shallow ion well.

[c7] 7.The EERPOM according to claim 6 wherein said first conductivity type is N type and said second conductivity type is P type.

[c8] 8.The EERPOM according to claim 6 wherein said stacked gate of said memory transistor comprises a floating gate and a control gate stacked on said floating gate.

[c9] 9.The EERPOM according to claim 8 wherein said control gate of said memory transistor is electrically connected to a word line.

[c10] 10.The EERPOM according to claim 6 wherein during said read operation, a positive read voltage is applied on said source line, and said deep ion well is grounded.

[c11] 11.An electrically erasable programmable read only memory (EERPOM) with source line voltage stabilization mechanism, comprising:
a semiconductor substrate of a first conductivity type having a memory region;
a deep ion well of a second conductivity type formed in said semiconductor substrate;
a cell ion well of said first conductivity type located within said memory region in said semiconductor sub-

strate, said cell ion well being situated above said deep ion well;

a shallow ion well of said second conductivity type serving as a buried bit line doped within said cell ion well, said shallow ion well being isolated by an STI layer, wherein said STI layer has a thickness greater than a well depth of said shallow ion well;

at least one memory cell block comprising a plurality of serially connected memory cells formed on said shallow ion well;

a selection transistor formed on said shallow ion well at one end of said memory cell block, said selection transistor has a first terminal serially connected to said memory cell block, and said selection transistor comprising a select gate and a second terminal electrically coupled to a source line, wherein said source line is further electrically coupled to said cell ion well to induce a capacitor between said cell ion well and said deep ion well during a read operation, thereby avoiding read current bounce or potential power crash; and

a bit line overlying said memory cell block and electrically connected to a drain of one of said plurality of serially connected memory cells at the other end of said memory cell block via a bit line contact plug short-circuiting said drain and said shallow ion well.

[c12] 12.The EERPOM according to claim 11 wherein said first conductivity type is N type and said second conductivity type is P type.

[c13] 13.The EERPOM according to claim 11 wherein each of said plurality of serially connected memory cells of said memory cell block comprises a floating gate and a control gate stacked on said floating gate.

[c14] 14.The EERPOM according to claim 13 wherein said control gate of said memory transistor is electrically connected to a word line.

[c15] 15.The EERPOM according to claim 11 wherein during said read operation, a positive read voltage is applied on said source line, and said deep ion well is grounded.